What is Claimed is:

1. A semiconductor device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a thyristor, and

an electrode disposed over a region of the thyristor; and

a bias circuit to bias the electrode with a voltage level dependent on temperature.

2. The device of claim 1, in which

the electrode is capacitively coupled to a base region of the thyristor; and

the bias circuit to sense a temperature and vary a voltage of the electrode based on the temperature sensed.

3. The device of claim 2, further comprising:

supporting material comprising at least one of semiconductor and conductor material;

insulating material over the supporting material;

the thyristor formed in a layer of silicon disposed over the insulating material;

dielectric disposed between the electrode the layer of silicon;

the bias circuit to define the voltage for the electrode relative to that of the supporting material.

4. The device of claim 1, the thyristor comprising:

a layer of silicon disposed in insulated relationship over a supporting substrate;

the thyristor comprising N-P-N-P doped regions in the layer of silicon for respective cathode-emitter, P-base, N-base and anode-emitter regions of the thyristor;

the electrode capacitively coupled to one of the N-base and P-base regions; and

the bias circuit to adjust the bias of at least one of the electrode and the supporting substrate

dependent on the temperature.

5. The device of claim 4, the bias for the electrode to influence carriers in the base region therebelow dependent on the temperature sensed.

6. The device of claim 1, the bias circuit to influence a gain of a bipolar device of the thyristor dependent on the temperature.

7. The device of claim 6, further comprising:

a support substrate comprising at least one of semiconductor and conductive material;

dielectric over the support substrate;

a layer of silicon over the dielectric;

doped regions in the layer of silicon defining the thyristor;

the bias circuit comprising:

temperature sensor to sense a temperature; and

a variable source to source a voltage level for the bias of at least one of the electrode and the support substrate based on the temperature sensed.

8. A thyristor memory device, comprising:

a thyristor formed in semiconductor material, the thyristor comprising:

an anode/cathode,

a cathode/anode, and

first and second base regions disposed in contiguous series relationship between the anode/cathode and the cathode/anode,

an electrode over one of the first and second base regions and operable under bias to affect an electric field therein;

a temperature dependent bias circuit to bias the electrode with a voltage dependent on

temperature.

9. The device of claim 8, the temperature dependent bias circuit to sense a temperature and establish the bias for the electrode with one of a positive or negative voltage-temperature coefficient of dependency.

10. The device of claim 9, further comprising:

a supporting substrate comprising silicon;

oxide over the supporting substrate;

a layer of silicon over the oxide;

the thyristor formed in at least a portion of the layer of silicon; and

dielectric between the electrode and the layer of silicon;

the temperature dependent bias circuit to sense a temperature and set the bias level of at least one of the electrode and the supporting substrate based on the temperature sensed.

11. The device of claim 8, in which

the thyristor comprises a bipolar transistor comprising a gain (beta) that is dependent on temperature with a first gain-versus-temperature coefficient of dependency;

the temperature dependent bias circuit to change the bias level of the electrode dependent on temperature to affect the gain of the bipolar transistor with a second gain-versus-temperature coefficient of dependency; and

the second gain-versus-temperature coefficient of dependency to counter the first gain-versus-temperature coefficient of dependency.

12. A semiconductor memory comprising:

an access transistor comprising a gateable channel;

a capacitively-coupled thyristor memory cell accessible via the access transistor;

the capacitively-coupled thyristor comprising a capacitor electrode disposed over a base region of the thyristor, and

a temperature sensing circuit to sense a temperature and affect a voltage of the capacitor electrode based on the temperature sensed.

13. The memory of claim 12, in which

the capacitively-coupled thyristor memory cell is formed in a silicon layer of an SOI substrate;

the temperature sensing circuit to define the voltage level of the capacitor electrode relative to that of a support substrate beneath the SOI structure.

14. A method of operating a thyristor-based memory device, comprising:

biasing an electrode disposed over a base region of a thyristor; and

sensing a temperature; and

influencing the biasing of the electrode based on the temperature sensed.

15. The method of claim 14, the influencing to define a voltage level of the electrode relative to that of a support substrate beneath the base region.

16. The method of claim 14, the influencing to affect a gain of a bipolar transistor of the thyristor to counter an intrinsic gain-versus-temperature characteristic thereof.

17. A circuit comprising:

a plurality of memory cells;

at least on memory cell of the plurality of memory cells comprising:

a capacitively-coupled thyristor having anode-emitter, N-base, P-base and cathode-emitter regions;

an capacitor electrode disposed over one of the N-base and P-base regions; and

a variable source to bias the electrode with a voltage level that changes dependent on

temperature.

18. The method of claim 17, in which the variable source biases the electrode with a voltage level defined relative to a support body of the thyristor.

19. The method of claim 18, in which the variable source changes the voltage level of one of the electrode or the support body based on temperature.

20. The method of claim 19, the variable source to charge the voltage level of the electrode relative to a supporting substrate beneath the thyristor.

21. The method of claim 17, further comprising an access transistor to selectively access the thyristor.

22. The method of claim 17, the thyristor comprising a bipolar transistor;

the bipolar transistor comprising a intrinsic gain-versus-temperature interdependency of a positive/negative co-efficient; and

the variable bias to influence the gain for the bipolar transistor for a negative/positive interrelationship co-efficient component that is opposite the intrinsic gain-versus-temperature interrelationship.

23. A method comprising:

operating a capacitively-coupled thyristor memory; and

sensing a temperature; and

controlling a gain of a bipolar transistor of a thyristor of the capacitively-coupled thyristor memory based on the temperature sensed.

24. The method of claim 23, in which the controlling the gain comprises affecting a voltage level of an electrode over a base region of the thyristor dependent on the temperature sensed.

25. The method of claim 23, in which the controlling the gain comprises affecting a voltage level of a supporting substrate beneath the thyristor dependent on the temperature sensed.

26. The method of claim 25, the thyristor formed in a silicon layer of a silicon on insulator (SOI) structure on the supporting substrate, the affecting the voltage level to bias the supporting substrate to influence an electric field through the base region between the electrode and the supporting substrate.

27. A semiconductor memory device comprising:

a thyristor;

an electrode capacitively-coupled to one of the base regions of the thyristor; and

means for setting a bias level of the electrode dependent on temperature.

28. The device of claim 27, further comprising:

a supporting substrate; and

an insulating layer over the supporting substrate;

the thyristor comprises N-P-N-P doped regions in contiguous serial relationship in a layer of silicon over the insulating layer;

the N-P-N and the P-N-P sequences of the thyristor representative of respective bipolar transistors; and

the means for setting the bias level is to establish an electric field through the base region between the electrode and the supporting substrate, and to influence a gain of its respective one of the N-P-N and P-N-P bipolar transistors dependent on the temperature.

the means for setting the bias level is operable to influence the gain of the bipolar transistor based on temperature an compensate for an intrinsic gain versus temperature dependency thereof.